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No. 07-

IN THE

Supreme Court of the United States

MAURICE MITCHELL INNOVATIONS, L.P.,

Petitioner,

v.

INTEL CORPORATION,

Respondent.

ON PETITION FOR A WRIT OF CERTIORARI TO THE UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

PETITION FOR A WRIT OF CERTIORARI

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QUESTIONS PRESENTED

1. Whether the legal standard for surviving summary judgment requires the non-movant to prove the merits of its case, rather than proving only the existence of a genuine issue of material fact.

2. Whether a court may properly grant summary judgment of patent invalidity based upon its own understanding of the patent claims and specification, without reference to record evidence regarding the understanding of a person of skill in the art of the patent.

PARTIES TO THE PROCEEDINGS AND CORPORATE DISCLOSURE

Petitioner

Petitioner, Maurice Mitchell Innovations, L.P. ("Mitchell"), is a non-governmental corporate party organized as a Texas Limited Partnership. Mitchell has no parent company and no subsidiaries or affiliates that have issued shares to the public. Mitchell discloses that there are no publicly held companies which own 10% or more of Mitchell's stock.

Respondent

Respondent, Intel Corporation ("Intel"), is a non-governmental corporate party, organized as a Delaware corporation. Intel's stock is publicly traded under the NASDAQ Symbol, INTC. It is unknown to Petitioner whether or not there are any publicly held companies which own 10% or more of Intel's stock.

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Maurice Mitchell Innovations, L.P. ("Mitchell" or "Petitioner") respectfully petitions for a writ of certiorari to review the judgment of the United States Court of Appeals for the Federal Circuit.

OPINIONS BELOW

The opinion of the Court of Appeals for the Federal Circuit was entered on September 24, 2007 and is unreported. (App. A at 1a) The order denying the Petition for Panel Rehearing and Rehearing En Banc was entered on November 5, 2007 and is also unreported. (App. D at 38a) The decision of the district court was entered on November 22, 2006 and is unreported. (App. B at 13a)

JURISDICTION

The Court of Appeals entered its judgment on September 24, 2007 (App. A at 1a) and denied the Petition for Panel Rehearing and Rehearing En Banc on November 5, 2007. (App. D at 38a) The jurisdiction of this Court is invoked under 28 U.S.C. § 1254(1) to review the Court of Appeals' decision on writ of certiorari.

CONSTITUTIONAL AND STATUTORY PROVISIONS INVOLVED

I. Supreme Court Rules 10(a) and 10(c):

> Review on a writ of certiorari is not a matter of right, but of judicial discretion. A petition for a writ of certiorari will be granted only for compelling reasons. The following, although neither controlling nor fully measuring the Court's discretion, indicate the character of the reasons the Court considers:
>
> > (a) a United States court of appeals has entered a decision in conflict with the decision of another United States court of appeals on the same important matter; has decided an important federal question in a way that conflicts with a decision by a state court of last resort; or has so far departed from the accepted and usual course of judicial proceedings, or sanctioned such a departure by a lower court, as to call for an exercise of this Court's supervisory power;
> >
> > * * * *
> >
> > (c) a state court or a United States court of appeals has decided an important question of federal law that has not been, but should be, settled by this Court, or has decided an important federal question in a way that conflicts with relevant decisions of this Court.

II. Federal Rule of Civil Procedure 56(c), which reads, in relevant part:

> The judgment sought should be rendered if the pleadings, the discovery and disclosure materials on file, and any affidavits show that there is no genuine issue as to any material fact and that the movant is entitled to judgment as a matter of law.

III. 35 U.S.C. § 112, ¶ ¶ 1, 2, and 6 of the Patent Act, which provides:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable **any person skilled in the art** to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention. (emphasis added)
>
> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
>
> * * * *
>
> An element in a claim for a combination may be expressed as a means or step for performing a specified function without the

recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.

STATEMENT OF THE CASE

This case presents two important questions of federal law. First, whether the legal standard for surviving summary judgment requires the non-movant to prove the merits of its case, rather than proving only the existence of a genuine issue of material fact. Second, whether a court may properly grant summary judgment of patent invalidity based upon its own understanding of the patent claims and specification, without reference to record evidence regarding the understanding of a person of ordinary skill in the art of the patent. The Court of Appeals for the Federal Circuit delivered an opinion in this matter wholly incongruous with the precedent of this Court on both questions. If the decision of the Court of Appeals for the Federal Circuit is not reversed, it will provide a blueprint to enable any jurist, on summary judgment, to invalidate a U.S. patent solely on the basis of attorney argument.

The Court of Appeals for the Federal Circuit affirmed the grant of summary judgment of invalidity of Petitioner's patent, holding that Petitioner had failed under 35 U.S.C. § 112 ¶ 2 and ¶ 6 to disclose sufficient structure in the specification to enable a means plus function limitation in Claim 1 of the patent. In doing so, the Court of Appeals erred.

First, the Court of Appeals failed to follow the well-established precedent of this Court controlling the determination of a motion for summary judgment by inquiring not whether a question of material fact existed, but whether the Petitioner, the non-moving party, proved that the patent specification disclosed sufficient structure to describe corresponding means-plus-function claim language. Second, the Court of Appeals improperly applied the precedent of this Court regarding the understanding of a person of ordinary skill in the art in the judicial determination of patent validity by substituting the Court's own understanding of the patent specification in place of the understanding of one skilled in the art.

The consequences of the Court of Appeals' ruling are to raise the burden of persuasion for a non-movant in summary judgment to equal the burden of persuasion at trial; to eviscerate the presumption of validity of all existing U.S. patents; and to undermine the precedent of this Court regarding summary judgment proceedings. Further, the Court's ruling shakes the foundation of U.S. patent jurisprudence as established by this Court in *Graham v. John Deere Co.*, 383 U.S. 1 (1966), and its progeny, by allowing the determination of patent validity to be viewed from the understanding of a layman rather than a person of ordinary skill in the art of the patent. This ruling – by the court assigned the duty of reviewing all patent litigation appeals – creates a glaring uncertainty for *every* U.S. patent owner and stands to chill the willingness of patent owners to pursue the enforcement of their rights through the judicial process.

In short, the decision of the Court of Appeals for the Federal Circuit allows a trial court, on summary judgment, to invalidate *any* patent that it does not understand, without regard to expert testimony or other record evidence regarding the technology of the patent. In view of the importance of this issue to every existing United States patent, this Court should review the Court of Appeals' decision.

REASONS FOR GRANTING THE PETITION

I. The Court Of Appeals' Decision Is Contrary To This Court's Precedent Regarding The Proper Standard For Summary Judgment

This Court's holding in *Anderson v. Liberty Lobby, Inc.*, 477 U.S. 242, 106 S. Ct. 2505 (1986), has long stood as the standard for summary judgment. The teaching of its precedent is clear.

> Rule 56(c) of the Federal Rules of Civil Procedure provides that summary judgment 'shall be rendered forthwith if the pleadings, depositions, answers to interrogatories, and admissions on file, together with the affidavits, if any, show that there is no genuine issue as to any material fact and that the moving party is entitled to a judgment as a matter of law.'

Id. at 477 U.S. at 247, 106 S. Ct. at 2509-10.

"In the . . . context of summary judgment under Rule 56 . . . the court must review the record 'taken as a whole.'" *Reeves v. Sanderson Plumbing Products, Inc.*, 530 U.S. 133, 150, 120 S. Ct. 2097, 2110 (2000) (quoting

Matsushita Elec. Industrial Co. v. Zenith Radio Corp., 475 U.S. 574, 587, 106 S. Ct. 1348, 89 L. Ed. 2d 538 (1986)). That is, "the court should review all of the evidence in the record," *Id.*, when considering a motion for summary judgment. "[T]he [non-movant], to survive the . . . motion, need only present evidence from which a jury might return a verdict in his favor. If he does so, there is a genuine issue of fact that requires a trial." *Anderson* at 477 U.S. at 257, 106 S. Ct. at 2514. "The evidence of the non-movant is to be believed, and all justifiable inferences are to be drawn in his favor." *Id.* at 477 U.S. at 255, 106 S. Ct. at 2513.

a. The Court of Appeals Failed to Draw All Reasonable Inferences in Favor of Petitioner, The Non-Movant

As stated, this Court's holding in *Anderson* instructs that in ruling on summary judgment, "[t]he evidence of the non-movant is to be believed, and all justifiable inferences are to be drawn in his favor." *Id.* at 477 U.S. at 255, 106 S. Ct. at 2513. "If reasonable minds could differ as to the import of the evidence, however, a verdict should not be directed." *Id.* at 477 U.S. at 250-1, 106 S. Ct. at 2511. In the present case, Petitioner Mitchell presented evidence sufficient to prove, literally as well as by reasonable inference, the validity of the '154 patent and the existence of a genuine issue of material fact requiring analysis by a jury. Contrary to the precedent of this Court, the Court of Appeals failed to draw such inferences in Petitioner Mitchell's favor. This clear departure from well-established precedent requires reversal of the Court of Appeals' affirmance of the trial court's grant of summary judgment.

Petitioner Mitchell offered as evidence the expert declaration of Dr. John D. Patterson, Ph.D. (App. C at 29a) In his declaration, Dr. Patterson unequivocally states that the specification of the '154 patent clearly and literally links the means plus function language "means for causing" to distinct structure in the form of the control elements of tri-state devices, which "were well known at the time that the patent application was filed." Decl. John D. Patterson, ¶ 5. (App. C at 31a) Further, through its reference to, and incorporation by reference of, the MCS6520 peripheral interface adapter and the MCS650X exemplary CPU, the specification disclosed to a person of ordinary skill at the time of the invention the use of the control elements of tri-state devices as the "specific structure" for causing the first and second switch means to remain in a non-signal conductive state. Decl. John D. Patterson, ¶ 5-7. (App. C at 31a-32a) Drawing all reasonable inferences in favor of Petitioner Mitchell, the non-movant, Dr. Patterson's declaration must be seen as accurately describing the knowledge of a person of skill in the art and such a person's reading of the '154 patent.

To simply disregard expert witness testimony that expressly states that the specification of the '154 patent properly and sufficiently discloses the structure associated with the "means for causing" to a person of skill in the art is to fail to draw *any* reasonable inference in Petitioner Mitchell's favor. This Court has said that when it fails to draw all reasonable inferences in favor of the non-moving party "the Court of Appeals impermissibly substitute[s] its judgment concerning the weight of the evidence for the jury's." *Reeves*, *supra*, 530 U.S. at 153, 120 S. Ct. at 2111. The Federal Circuit

Court of Appeals' refusal here to draw inferences in favor of Petitioner Mitchell is wholly contrary to the precedent of this Court. As a result, the decision of the Court of Appeals, affirming the grant of summary judgment should be reversed.

b. The Decisions Below Confuse Petitioner's Evidentiary Burden in Withstanding a Motion for Summary Judgment with the Standard of Proof Required at Trial and Conflict with the Well-Established Precedent of this Court

> [T]he issue of material fact required by Rule 56(c) to be present to entitle a party to proceed to trial is not required to be resolved conclusively in favor of the party asserting its existence; rather, all that is required is that sufficient evidence supporting the claimed factual dispute be shown to require a jury or judge to resolve the parties' differing versions of the truth at trial.

Anderson at 477 U.S. at 248-9, 106 S. Ct. at 2510 (quoting *First National Bank of Arizona v. Cities Service Co.*, 391 U.S. 253, 288-9, 88 S. Ct. 1575, 1592 (1968)).

In its decision below, the Federal Circuit Court of Appeals, in affirming the grant of summary judgment, performs its own analysis of the '154 patent and its specification, unassisted by competent expert testimony or other evidence, and concludes that Petitioner Mitchell "does not carry out its part of the quid pro quo bargain [for using means plus function claim language]. [The Court of Appeals] sustains the finding that claim 1 is

indefinite under [*sic* 35] U.S.C. § 112, ¶ 2." (App. A at 11a) The Court of Appeals in its holding clearly has undertaken to determine the case on its merits, confusing its function in reviewing a grant of summary judgment and running afoul of the direction of this Court regarding the burden to be carried by the non-movant in summary judgment proceedings.

The Court of Appeals wrote that the district court "correctly found the specification did not contain any corresponding structure for [the "means for causing"] limitation." (App. A at 12a) Petitioner Mitchell, as is required by the standard of summary judgment, has presented a genuine issue of material fact, which the courts below have improperly attempted to resolve conclusively. The existence of the question itself meets the burden required to survive summary judgment. In basing their opinions upon weighing the merits of the case in chief, both courts below confuse the burden of surviving summary judgment with the standard of proof at trial. The judgment of the courts below, based upon this error, conflicts with both Federal Rule 56 and the precedent of this Court and should be reversed so that the questions addressed below may properly be submitted to a jury for consideration.

c. The Decisions Below Ignored Unrebutted Evidence that Demonstrates that a Genuine Issue of Material Fact Exists

In its September 24, 2007 opinion, (App. A at 1a) the Court of Appeals makes not a single mention of the evidence presented by Petitioner Mitchell in the expert report of Dr. John D. Patterson, Ph.D. (App. C at 29a)

This report expresses the understanding of persons of skill in the art of digital microprocessor architecture at the time the '154 patent was issued. In his declaration, Dr. Patterson testifies that "there is sufficient disclosure to one skilled in the art what structure is used to perform the function of the elements 13 and 14 of the claim which call for [13] 'means for causing.'" Decl. John D. Patterson, Ph.D. at ¶ 3. (App. C at 30a) Dr. Patterson continues:

> [t]he knowledge of one skilled in the art when interpreting the statement at col 15, lines 61-63 . . . would be sufficient to determine that the structure of the 'means for causing' provided by the interface circuits containing tri-state devices is taught by the referenced technical description of the MCS6520 PIA, which was well known to persons of ordinary skill in the art at the time of the invention.

Id. at ¶ 10. (App. C at 33a)

Dr. Patterson concludes:

> The description of the functions of the means for causing in limitations 13 and 14 is a description of the function of the first and second switch means. That is what is described in Col. 24, line 67 to Col. 25, line 56. One skilled in the art would understand the structure of the switch means that is used for the means for causing in limitations 13 and 14 of the claim is the control element structure taught by the

> tri-state devices of the MCS6520 which as set forth above, are examples of the tri-state logic circuit structure.

Id. at ¶ 18. (App. C at 36a)

Respondent Intel presented no contradictory expert testimony, nor any other evidence to rebut Dr. Patterson's declaration. Even if Respondent Intel had done so, this evidence was required to be construed in the light most favorable to Petitioner, the non-movant. As this Court stated most recently in *KSR v. Teleflex*, 127 S. Ct. 1727, 1745 (2007), "[i]n considering summary judgment . . . the district court can and should take into account expert testimony, which may resolve or keep open certain questions of fact." Instead, the district court and the Court of Appeals wholly disregarded this evidence.

> In *Daubert v. Merrell Dow Pharmaceuticals, Inc.*, 509 U.S. 579, 113 S.Ct. 2786, 125 L.Ed.2d 469 (1993), the Supreme Court assigned to trial courts the responsibility of determining whether expert testimony under Rule 702 is 'not only relevant, but reliable.' *Id.* at 589, 113 S.Ct. 2786. In this gate-keeping role, trial courts make 'a preliminary assessment of whether the reasoning or methodology underlying the testimony is scientifically valid and of whether that reasoning or methodology properly can be applied to the facts in issue.' *Id.* at 592-93, 113 S.Ct. 2786.

Hathaway v. Bazany, 2007 WL 3200413 at *3 (5th Cir. November 1, 2007). Here, the Federal Circuit Court of

Appeals made no such preliminary assessment, nor did Respondent Intel provide an iota of evidence to question the reliability of the expert testimony offered. Based upon this fact and the well-established rule that the evidence of the non-movant on a motion for summary judgment must be viewed in the light most favorable to him, it was inappropriate for the Federal Circuit Court of Appeals to ignore Petitioner Mitchell's expert evidence and likewise inappropriate for the Federal Circuit Court of Appeals to affirm the grant of summary judgment when that evidence and all justifiable inferences therefrom clearly create a genuine issue of material fact that must be resolved by a jury.

While *Daubert* permits the lower courts broad discretion in determining the admissibility and sufficiency of expert testimony, that testimony may not be wholly ignored. "In the . . . context of summary judgment under Rule 56 . . . the court must review the record 'taken as a whole' . . . [and] the court should review *all* of the evidence in the record." *Reeves*, *supra*, 530 U.S. at 150, 120 S. Ct. at 2110 (emphasis added). Neither the Court of Appeals for the Federal Circuit nor the district court reviewed the record as a whole. Each ignored the unrebutted evidence of Petitioner Mitchell's expert and, by extension, necessarily failed to draw all justifiable inferences from that evidence in favor of Petitioner Mitchell.

In his concurring opinion in *Celotex Corp. v. Catrett*, Justice White wrote that if the non-movant "has named a witness to support [his] claim, summary judgment should not be granted without [the movant] somehow showing that the named witness' possible testimony

raises no genuine issue of material fact." 477 U.S. 317, 328, 106 S. Ct. 2548, 2555 (1986) (White, J. concurring). Respondent Intel has made no such showing, nor even attempted to do so. Bald assertions and attorney argument cannot dispatch the evidence presented by Petitioner Mitchell's expert and certainly does not relieve the Court of Appeals of its duty to consider the existence of such evidence in reviewing the trial court's grant of summary judgment. The Court of Appeals for the Federal Circuit, however, failed to give Petitioner Mitchell's expert witness evidence any review.

This Court has held in similar circumstances that such disregard of relevant evidence is grounds for reversal of summary judgment. Here, as in *Toyota Motor Mfr. v. Williams*, "the Court of Appeals appears to have disregarded the very type of evidence that it should have focused on." 534 U.S. 184, 201, 122 S. Ct. 681, 693 (2002). "[I]t was therefore inappropriate for the Court of Appeals to grant . . . summary judgment . . . on the issue . . . and its decision to do so must be reversed." *Id.* at 534 U.S. at 202, 122 S. Ct. at 694.

II. The Court Of Appeals' Failure To Consider The Understanding Of A Person Of Ordinary Skill In The Art Is Inconsistent With The Precedent Of This Court

a. The Court of Appeals Substituted Its Own Understanding for the Understanding of a Person of Ordinary Skill in the Art

The Court of Appeals for the Federal Circuit wrote in its opinion in the present matter, "[i]t is important to determine whether one of skill in the art would understand the specification itself to disclose the structure [corresponding to means plus function language], not simply whether that person would be capable of implementing that structure." (quoting *Med. Instrumentation & Diagnostic Corp. v. Elekta AB*, 344 F.3d 1205, 1212 (Fed. Cir. 2003). (App. A at 10a) However, the Court of Appeals for the Federal Circuit undertook this analysis based upon its own understanding and reading of the specification, without reference to the only evidence of record, that of Petitioner Mitchell's expert, Dr. Patterson, and without regard to the understanding of one skilled in the art.

Based upon only the court's reading of the patent and attorney argument, without mention of Petitioner Mitchell's evidence regarding the understanding of a person of skill in the art, the Court of Appeals for the Federal Circuit wrote "this court has examined these passages [of the patent specification] and finds no specific structure." *Id.* (App. A at 10a) The Court of Appeals' opinion ignores the requirement of this Court's precedent that the specification be read with the understanding of a person of ordinary skill in the

relevant art. As such, the Court of Appeals' affirming the grant of summary judgment was improper and should be reversed so that evidence regarding the understanding of a person of ordinary skill may be considered and a judgment rendered in accordance with the precedent of this Court.

The need for expert testimony regarding the understanding of a person of skill in the art of a patent has been well elucidated in patent litigation in the context of obviousness. Judge Learned Hand wrote:

> The test laid down is indeed misty enough. It directs us to surmise what was the range of ingenuity of a person 'having ordinary skill' in an 'art' with which we are totally unfamiliar; and we do not see how such a standard can be applied at all except by recourse to the earlier work in the art, and to the general history of the means available at the time. To judge on our own that this or that new assemblage of old factors was, or was not, 'obvious' is to substitute our ignorance for the acquaintance with the subject of those who were familiar with it.

Reiner v. I. Leon Co., Inc., 285 F.2d 501, 503-4 (2nd Cir. 1960). To assert that the need for expert testimony to establish the standard of knowledge of a person of skill in the art is any different whether the legal inquiry is obviousness or – as it is here – indefiniteness is but sleight of hand. This court agreed and in its landmark opinion in *Graham v. John Deere Co.* cited Judge Hand's opinion in *Reiner*, adding that the judiciary "is most ill-

fitted to discharge the technological duties cast upon it by patent litigation." 383 U.S. 1, 36, 86 S. Ct. 684, 703 (1966). Likewise, commentators have observed that "it is not surprising that trial judges in many cases find difficulty in understanding the innovations, the briefs, and the exhibits" in patent litigation. Note, *Subtests of "Nonobviousness": A Nontechnical Approach to Patent Validity*, 112 U. Pa. L. Rev. 1169 (1964). This Court also agreed with that assessment, citing it in *Graham*.

The Court of Appeals in this case has in fact resorted to its own knowledge regarding the state of the art of digital microprocessor design, as it existed over 24 years ago (as the Mitchell '154 patent claims a filing date referring back to October 13, 1983), rather than looking to the expert testimony of persons qualified to explicate such understanding at that time. The Court of Appeals wrote that it "discerns little, if any, structure for 'means for causing' in the specification and no disclosed link between that purported structure and the claimed function." (App. A at 9a) At the same time, the sole uncontroverted evidence in the record states that "there is sufficient disclosure to one skilled in the art what structure is used to perform the function of the . . . 'means for causing.'" Decl. of John D. Patterson, ¶ 3. (App. C at 30a) Specifically, Dr. Patterson stated that the structure of the "means for causing" is the control elements of tri-state circuits. The Court of Appeals clearly substitutes its own unfamiliarity with the subject for the understanding of an expert in the field. By this, the Court of Appeals impermissibly redefined the inquiry into patent validity as at trial, rather than in summary judgment. The Court of Appeals for the Federal Circuit's holding is incongruous with the precedent of this Court and should be reversed.

b. The Supreme Court Should Use Its Supervisory Powers To Preclude The Court of Appeals From Not Following This Court's Mandate

"This Court has supervisory authority over the federal courts, and [it] may use that authority to prescribe rules of evidence and procedure that are binding in those tribunals." *Dickerson v. United States*, 530 U.S. 428, 437, 120 S. Ct. 2326, 2332 (2000) (citing *Carlisle v. United States*, 517 U.S. 416, 426, 116 S. Ct. 1460, 134 L. Ed. 2d 613 (1996)). In codifying and exercising its supervisory power, this Court has promulgated Supreme Court Rule 10, stating that the Court may find reason to review an appellate court's decision when that decision has "departed from the accepted and usual course of judicial proceedings, or sanctioned such a departure by a lower court" or where "a United States court of appeals . . . has decided an important federal question in a way that conflicts with relevant decisions of this Court." As expressed in the foregoing pages, the trial court in this case has departed from the usual course of judicial proceedings and deviated from the relevant precedent of this Court with regard to the standard of summary judgment and the understanding of a person of ordinary skill in the art. With respect to both questions, the Court of Appeals for the Federal Circuit affirmed the trial court's grant of summary judgment, thereby sanctioning these departures and joining in their deviation from this Court's prior decisions. These departures call for review by this Court in the exercise and maintenance of its supervisory powers.

This Court formulated its rules of procedure and evidence guided by basic considerations of justice. *McNabb v. United States*, 318 U.S. 332, 340 (1943). Thus, the Court's supervisory powers go beyond merely maintaining due process. However, this Court's pronouncements of the standards of justice and precedent cannot be duly upheld where appellate and trial courts can, based upon their own understanding, choose not to follow the summary judgment mandates and patent law pronouncements of this Court. In the present matter, this is precisely what the Court of Appeals for the Federal Circuit has done during its appellate review.

Consequently, the Court is respectfully requested to exercise its supervisory powers and maintain the proper standards of jurisprudence by instructing the Federal Circuit to follow this Court's holdings in *Anderson, supra*, and its progeny, as it relates to summary judgment rules, and *Graham v. John Deere Co., supra*, as it relates to persons of ordinary skill in the art.

CONCLUSION

For the foregoing reasons, the Petition for a Writ of Certiorari should be granted.

Respectfully submitted,

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APPENDIX

APPENDIX A — OPINION OF THE UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT, DECIDED SEPTEMBER 24, 2007

UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

2007-1108

MAURICE MITCHELL INNOVATIONS, L.P.,

Plaintiff-Appellant,

v.

INTEL CORPORATION,

Defendant-Appellee.

DECIDED: September 24, 2007

Before RADER, MOORE, *Circuit Judges*, and YEAKEL, *District Judge**.

RADER, *Circuit Judge*.

The United States District Court for the Eastern District of Texas granted Intel Corporation's ("Intel") motion for summary judgment that claim 1 of U.S. Patent No. 4,875,154 ("the '154 patent") is invalid as indefinite

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* Honorable Lee Yeakel, District Judge, United States District Court for the Western District of Texas, sitting by designation.

pursuant to 35 U.S.C. § 112, ¶ 2. *Maurice Mitchell Innovations, L.P. v. Intel Corp.*, No. 2:04-CV-450 (E.D.Tex. Dec. 11, 2006) (" *Final Judgment* "); *Maurice Mitchell Innovations, L.P. v. Intel Corp.*, No. 2:04-CV-450 (E.D.Tex Nov. 22, 2006 (" *Opinion* "); *Maurice Mitchell Innovations, L.P. v. Intel Corp.*, No. 2:04-CV-450 (E.D.Tex. Jun. 21, 2006) ("*Claim Construction Opinion* "). Because the district court correctly construed the claim term "means for causing" as a means-plus-function limitation under 35 U.S.C. § 112, ¶ 6 and correctly found the specification did not contain any corresponding structure, this court affirms.

I

The United States Patent and Trademark Office issued the '154 patent, entitled Microcomputer with Disconnected, Open, Independent, Bimemory Architecture, Allowing Large Interacting, Interconnected Multi-microcomputer Parallel Systems Accomodating [sic] Multiple Levels of Programmer Defined Heirarchy [sic], on October 17, 1989 from an application filed on June 12, 1987. The patent abstract states:

> A Bimemory Independent CPU (BICPU) microcomputer which is comprised of a known CPU chip provided with additional circuitry to enable CPU to interact in a multi BICPU microcomputer system. Each BICPU microcomputer in a system is supplied with an assigned standard memory mechanically

> and logically connected to it's [sic] BICPU's "A" bus circuits. The BICPU microcomputer is also provided with connectors enabling the CPU to be connected to system buses. Any number of BICPU microcomputers can be logically chained, linked and treed in a simple logical bimemory independent pattern infinitely in as many dimensions as is reasonably desired, using one standard set of dedicated, simple, single line conductors (system buses) to mechanically interconnect any "B" or "C" bus curcuits [sic] of two different BICPU microcomputers.

'154 Patent Abstract. Generally, the patent describes a BICPU computer system "comprised of a known CPU chip with additional circuitry to enable the CPU to interact in a multi BICPU microcomputer system." '154 Patent col.7 ll.3-6. According to the specification, the invention allows "[a]ny number of BICPU microcomputers [to] be logically chained, linked and treed in a simple logical bimemory independent pattern infinitely in as many dimensions as is reasonably desired, using one standard set of dedicated, simple, single line conductors (system buses) to mechanically interconnect any 'B' or 'C' bus circuits of two different BICPU microcomputers." '154 Patent col.7 ll.12-19. Claim 1 reads:

Appendix A

A microcomputer data processing apparatus, comprising:

[1] a Central Processing Unit (CPU),

[2] *a path configuring means*,

[3] path control circuits connecting said CPU to said *path configuring means*,

[4] a plurality of contacts comprised of a plurality of distinct sets,

[5] wherein said CPU further comprises a dedicated memory address circuit, a dedicated memory data circuit, a dedicated memory control circuit and a dedicated power circuit,

[6] wherein said *path configuring means* further comprises a dedicated memory address circuit, a dedicated memory data circuit and a dedicated memory control circuit,

[7] wherein each dedicated memory address, data, and control circuit includes a plurality of dedicated memory address, data, and control lines respectively, wherein

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[8] said memory control lines are comprised of a read/write line, timing lines and status lines,

[9] first *switch means* comprised of at least three distinct parts of connecting said dedicated memory address, data, and control circuits of said *path configuring means* to each of said first three sets of contacts, and

[10] second *switch means* for connecting said dedicated memory address, data, and control lines of said *path configuring means* to said dedicated memory address, data, and control lines of said CPU respectively,

[11] wherein said first and second *switch means* assume a non signal-conducting state when said CPU power circuit is not supplied with power,

[12] wherein said lines of said CPU an said contacts assume a non-signal conducting state when said first and second *switch means* are in said non-signal conducting state,

[13] *means for causing* said first and second *switch means* to remain in said non signal-conducting state upon application of

power to said CPU power circuit and to assume a signal-conductive state upon receipt of an appropriate signal from said CPU, and to

[14] assume a non signal-conducting state upon receipt of an appropriate signal from said CPU.

'154 Patent col.90 l.59-col.91 l.37 (emphases and [limitation numbers] added).

Maurice Mitchell Innovations, L.P. ("Mitchell") brought suit against Intel in the United State District Court for the Eastern District of Texas alleging a number of Intel's products infringe Claim 1 of the '154 patent. In construing the claims, the district court adopted the claim construction of District Judge Susan Illston of the United States District Court for the Northern District of California. *Claim Construction Opinion; see, Maurice Mitchell v. Samsung Electronics Co., Ltd.*, No. C 01-0295 SI (N.D.Cal. Jan. 29, 2002). Specifically, the district court construed "first switch means," "second switch means," and "means for causing" as means-plus-function limitations governed by 35 U.S.C. § 112, ¶ 6. *Id.* The district court then determined that the '154 patent specification did not disclose structure for the "switch means" limitations and the "means for causing" limitation. *Opinion.* As a result, the district court found Claim 1 of the 2154 patent indefinite and therefore invalid as a matter of law. *Id.*

II

This court reviews a district court's grant of summary judgment without deference, drawing all justifiable inferences in favor of the nonmovant. *Genentech, Inc. v. Amgen, Inc.*, 289 F.3d 761, 767 (Fed.Cir.2002). Claim construction is a matter of law that this court reviews without deference. *Cybor Corp. v. FAS Techs., Inc.*, 138 F.3d 1448, 1456 (Fed.Cir.1998) (en banc); *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed.Cir.1995), *aff'd*, 517 U.S. 370, 116 S.Ct. 1384, 134 L.Ed.2d 577 (1996). "The review of indefiniteness under 35 U.S.C. § 112, paragraph 2, proceeds as a question of law without deference." *SmithKline Beecham Corp. v. Apotex Corp.*, 403 F.3d 1331, 1338 (Fed.Cir.2005).

"A patent issued from the United States Patent and Trademark Office (PTO) bears the presumption of validity under 35 U.S.C. § 282. An accused infringer, therefore, must prove patent invalidity under the clear and convincing evidentiary standard." *Metabolite Labs., Inc. v. Lab. Corp. of Am. Holdings*, 370 F.3d 1354, 1365 (Fed.Cir.2004). Specifically, "[t]he claims as granted are accompanied by a presumption of validity based on compliance with, inter alia, § 112 ¶ 2." *S3 Inc. v. NVIDIA Corp.*, 259 F.3d 1364, 1367 (Fed.Cir.2001).

As stated in § 112 ¶ 2, "[t]he specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention." Claims "particularly

point[ ] out and distinctly claim[ ]" the invention when one of ordinary skill in the art would understand the scope of the invention when the claims are read in conjunction with the specification. *Default Proof Credit Card Sys., Inc. v. Home Depot U.S.A., Inc.*, 412 F.3d 1291, 1298 (Fed.Cir.2005); 35 U.S.C. § 112 ¶ 2. But, if an applicant "employs means-plus-function language in a claim, one must set forth in the specification an adequate disclosure showing what is meant by that language." *In re Donaldson*, 16 F.3d 1189, 1195 (Fed.Cir.1994) (en banc); 35 U.S.C. § 112 ¶ 6. Therefore, "[i]f there is no structure in the specification corresponding to the means-plus-function limitation in the claims, the claim will be found invalid as indefinite." *Biomedino, LLC v. Waters Technologies Corp.*, 490 F.3d 946, 950 (Fed.Cir.2007).

III

The district court found that "means for causing" was a means-plus-function limitation without any descriptive corresponding structure within the specification. The only possible structure corresponding to the claimed function appears at Col.24 l.67 to Col.25 l. 56. *Opinion*, slip op. at 8. The district court then determined this passage did not contain any structure.

As illustrated by the claim language in limitation 13, the "means for causing" controls the first and second switch means. In other words, the "means for causing" would need a structure (i .e., device or driver) to control the function of the switch means. Mitchell contends that

the '154 patent specification contains an adequate disclosure corresponding to the "means for causing" limitation to satisfy § 112 ¶ 2. Mitchell argues that the district court incorrectly limited the corresponding structure to the disclosure at Col.24 l.67 to Col.25 l.56 when the following additional passages also disclose structure: Col.15, ll.40-56; Col.19, line 34 to Col.20, line 5; Col.13, ll.11-19; Col.7, ll.37-44; Col.44, ll.21-46; Col.89, ll.14-49; Col.90, ll.16-30; and Col.16, ll.48-53.

Like the district court, however, this court discerns little, if any, structure for "means for causing" in the specification and no disclosed link between that purported structure and the claimed function. This court also credits the district court's finding that Mitchell's counsel admitted during the summary judgment hearing that the Col.24 l.67 to Col.25 l.56 passage does not include any structure linked to the claimed function. *Maurice Mitchell Innovations v. Intel Corp.*, 2:04cv450, slip op. at 35 (E.D.Tex. Sept. 28, 2006) (Transcript of Pretrial and Motion Hearing). Beyond that passage, however, this court finds no specific structure disclosed anywhere in the specification to carry out the "means for causing" function.

Mitchell also offers another source of structure for the claimed means. The specification refers to the MCS6520 Peripheral Interface Adaptor ("PIA"). '154 Patent col.15 ll.40-55. The MCS6520 is a complex integrated circuit (i.e., chip) containing numerous individual circuits which functions as an interface between a microprocessor and peripheral devices such

as printers, displays and the like. Mitchell contends that the MCS6520 contains tri-state circuitry or tri-state drivers and that a person of ordinary skill in the art would understand the tri-state structure in the MCS6520 to be capable of performing the "means for causing" function.

While the MCS6520 may contain tri-state or driver type circuits, the specification does not identify the tri-state circuits in the MCS6520 as the structure to carry out the "means for causing" limitation. The mere mention of a complicated integrated circuit, comprised of hundreds if not thousands of circuits, is much too broad to sufficiently indicate the precise "means for causing" structure to a person of ordinary skill in the art. *See Med. Instrumentation & Diagnostic Corp. v. Elekta AB*, 344 F.3d 1205, 1212 (Fed.Cir.2003) ("It is important to determine whether one of skill in the art would understand the specification itself to disclose the structure, not simply whether that person would be capable of implementing that structure."). In other words, as the district court noted, the MCS6520 is both too broad and not linked to the "means for causing" limitation. *Opinion*, slip op. at 8-9.

Mitchell also attempts to identify structure in a variety of generalized passages in the specification. This court has examined these passages and finds no specific structure. Mitchell only states that "[t]hese passages are additional disclosures of the details of the structure, readily apparent to a person of ordinary skill in the art." In effect, Mitchell merely references various passages

in the specification without providing any information to show structure corresponding to "means for causing." Mitchell appears to be arguing that a person of ordinary skill in the art would be able to ascertain the corresponding structure by combining a variety of passages in the specification with their knowledge of the art. However, "in order for a claim to meet the particularity requirement of ¶ 2, the corresponding structure(s) of a means-plus-function limitation must be disclosed in the written description in such a manner that one skilled in the art will know and understand what structure corresponds to the means limitation." *Atmel Corp. v. Info. Storage Devices, Inc.*, 198 F.3d 1374, 1382 (Fed.Cir.1999). Thus, the statute requires more than just the possibility that an artisan of ordinary skill may be able to figure out the corresponding structure. The quid pro quo for using a means-plus-function limitation requires specificity in reciting structure and linking that structure to the limitation. *Id.* Mitchell does not carry out its part of the quid pro quo bargain. This court sustains the finding that claim 1 is indefinite under U.S.C. § 112, ¶ 2.

This court need not reach the "switch means" and "path configuring means" limitations because the district court's decision can be affirmed solely on the "means for causing" limitation.

IV

Because the district court correctly construed the claim term "means for causing" as a means-plus-function limitation under 35 U .S.C. § 112, ¶ 6 and correctly found the specification did not contain any corresponding structure for this limitation, this court affirms.

AFFIRMED

COSTS

Each party shall bear its own costs.

APPENDIX B — MEMORANDUM OPINION AND ORDER OF THE UNITED STATES DISTRICT COURT FOR THE EASTERN DISTRICT OF TEXAS, MARSHALL DIVISION, DATED NOVEMBER 22, 2006

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

CASE NO. 2:04-CV-450

MAURICE MITCHELL INNOVATIONS, L.P.,

Plaintiff

v.

INTEL CORPORATION,

Defendant

MEMORANDUM OPINION AND ORDER

Before the Court is Defendant Intel Corporation's ("Intel") motion for summary judgment as to invalidity under 35 U.S.C. § 112 (Docket No. 104). Having considered the parties' written submissions and oral argument, the Court **GRANTS** the motion.

Appendix B

BACKGROUND

Maurice Mitchell Innovations, L.P. ("Mitchell") filed suit against Intel on December 17, 2004 alleging infringement of Claim 1 of U.S. Patent No. 4,875,154 ("the '154 patent"). In general, the '154 patent discloses what the patent refers to as a "Bimemory Independent CPU ('central processing unit')" microcomputer, also referred to as a "BICPU microcomputer." According to the specification, the BICPU microcomputer

> is comprised of a known CPU chip with additional circuitry to enable the CPU to interact in a multi BICPU microcomputer system. Each BICPU microcomputer within a system is supplied with an assigned standard memory-mechanically and logically connected to its BICPU's "A" bus circuits. The BICPU microcomputer is also provided with connectors enabling the CPU to be connected to system buses.

Col. 7:3-12. In general terms, the specification says that the invention allows a number of BICPU microcomputers to be linked together in a "bimemory independent pattern" using a "standard" set of system buses to mechanically interconnect "B" or "C" bus circuits of any two BICPU microcomputers. Col. 7:12-22. Mitchell claims Intel's products, including *inter alia*, the ASCI Red super computers, the Pentium II, Pentium III, and Pentium IV processors, contain chipsets that infringe the '154 patent.

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At the *Markman* hearing, the Court construed Claim 1 limitations nine and ten,[1] and thirteen and fourteen[2] as means-plus-function terms and construed the functions of those terms. Intel argued at the hearing that there were no corresponding structures for these functions. At the hearing, Mitchell argued that the terms were not means-plus-function limitations. In order to be fully briefed on the issue of corresponding structure, the Court did not identify the corresponding structures for these functions and instead deferred the issue to summary judgment. The determination of whether a corresponding structure exists for these functions is now ripe for decision.

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1. Limitation nine states "first switch means comprised of at least three distinct parts for connecting said dedicated memory address, data, and control circuits of said path configuring means to each of said first three sets of contacts."

Limitation ten states "second switch means for connecting said dedicated memory address, data, and control lines of said path configuring means to said dedicated memory address, data, and control lines of said CPU respectively."

2. Limitations thirteen and fourteen state "means for causing said first and second switch means to remain in said non signal-conducting state upon application of power to said CPU power circuit and to assume a signal conductive state upon receipt of an appropriate signal from said CPU" and to "assume a non signal-conducting state upon receipt of an appropriate signal from said CPU."

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APPLICABLE LAW

Summary Judgment Standard

Summary judgment shall be rendered when the pleadings, depositions, answers to interrogatories, and admissions on file, together with the affidavits, if any, show that there is no genuine issue as to any material fact and that the moving party is entitled to judgment as a matter of law. Fed.R.Civ.P. 56(c); *Celotex Corp. v. Catrett*, 477 U.S. 317, 323-25 (1986); *Ragas v. Tenn. Gas Pipeline Co.*, 136 F.3d 455, 458 (5th Cir.1998). An issue of material fact is genuine if the evidence could lead a reasonable jury to find for the non-moving party. *Anderson v. Liberty Lobby, Inc.*, 477 U.S. 242, 248 (1986). In determining whether a genuine issue for trial exists, the court views all inferences drawn from the factual record in the light most favorable to the non-moving party. *Id.; Matsushita Elec. Indus. Co. v. Zenith Radio*, 475 U.S. 574, 587 (1986).

Indefiniteness

A patent is entitled to a presumption of validity, and an accused infringer must prove invalidity by clear and convincing evidence. *Metabolite Labs., Inc. v. Lab. Corp.*, 370 F.3d 1354, 1365 (Fed.Cir.2004). The requirement that "claims 'particularly point . . . out and distinctly claim . . .' the invention is met when a person experienced in the field of the invention would understand the scope of the subject matter that is patented when reading the claim in conjunction with the rest of the specification."

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Default Proof Credit Card Sys., Inc. v. Home Depot U.S.A., Inc., 412 F.3d 1291, 1298 (Fed.Cir.2005) (quoting *S3 Inc. v. nVIDIA Corp.*, 259 F.3d 1364, 1367 (Fed.Cir.2001)). However, if one " 'employs means-plus-function language in a claim, one must set forth in the specification an adequate disclosure showing what is meant by that language. If an applicant fails to set forth an adequate disclosure, the applicant has in effect failed to particularly point out and distinctly claim the invention as required by the second paragraph of section 112." *See* 35 U.S.C. § 112, ¶ 6." *Id.* (quoting *In Re Donaldson Co.*, 16 F.3d 1189, 1195 (Fed.Cir.1994) (en banc)).

Accordingly, when faced with means-plus-function limitations, courts "must turn to the written description of the patent to find the structure that corresponds to the means recited in the [limitations]." *Default*, 412 F.3d at 1298. " 'A structure disclosed in the specification qualifies as "corresponding" structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim.' " *Id.* (quoting *B. Braun Med. v. Abbott Labs.*, 124 F.3d 1419, 1424 (Fed.Cir.1997)). "This duty to link or associate structure to function is the *quid pro quo* for the convenience of employing § 112, ¶ 6." *Id.* (citing *O.I. Corp. v. Tekmar Co.*, 115 F.3d 1576, 1583 (Fed.Cir.1997)). The question is "whether one skilled in the art would understand the specification itself to disclose the structure, not simply whether that person would be capable of implementing that structure." *Med. Instrumentation & Diagnostics Corp. v. Elekta AB*, 344 F.3d 1205, 1212 (Fed.Cir.2003).

Appendix B

ANALYSIS

Corresponding Structure for First and Second Switch Means

The ninth limitation claims a "first switch means" with a function of "connecting said dedicated memory address, data, and control circuits of said path configuring means to each of said first three sets of contacts." Claim Construction Opinion at 32. The tenth limitation claims a "second switch means" with a function of "connecting said dedicated memory address, data, and control lines of said path configuring means to said dedicated memory address, data, and control lines of said CPU respectively." *Id.* at 33.

Mitchell asserts that the corresponding structure for these functions is described at columns 19:64-20:5. This passage says:

> Each first switch means, second switch means, third switch means 108, fourth switch means 110, fifth switch means 112, sixth switch means 114, and seventh switch means 116, it is noted, actually represents a plurality of logical elements, each of which can logically disconnect an address, data, or control circuit that is mechanically connected to the switch means, under the control of the CPU 102 when power is being supplied to the BICPU microcomputer power circuits.

'154 patent, col. 19:64-20:5. This passage merely refers to a "plurality of logical elements." Even Mitchell himself recognized that a plurality of logical elements can refer to any number of combinations of elements and does not refer to a specific structure.[3] Dr. Patterson, Mitchell's expert, corroborated Mitchell's testimony regarding this issue.[4]

At the hearing on this motion, the Court repeatedly asked Mitchell to identify a structure in the specification that corresponded to the functions.[5] Mitchell could only

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3. When asked in his deposition whether the patent described anywhere which of these thousands of "logical elements" should be used to build the first switch means, Mitchell responded "that leaves that up to the designers." Mitchell Depo. at 224:23-225:12. Mitchell further recognized that the switch means could be built in "almost as many different ways as there were design teams." *Id.*

4. When asked about how many possible combinations of circuits could provide this logical connection other than the tri-state device, Patterson responded "there is many other examples . . . [t]here is, you got all the combinations of all kinds of things that can be. It can be a big number, I don't know." Patterson Depo. at 155:8-25.

5. The transcript from the hearing at p. 26-27 states:

> **THE COURT:** So what are you saying, though, is the structure and is it supported by the summary judgment proof; and if so where?

(Cont'd)

point to the language above and tell the Court that a person skilled in the art would know that a "plurality of logical elements" necessarily referred to tri-state circuitry. Notably, tri-state circuitry is never mentioned the language quoted above, nor does it appear anywhere in the specification.

Mitchell argues that a person skilled in the art could read the function of limitations nine and ten and infer from the function that a tri-state circuitry device is *a* device that *could* perform the function. *See* Patters 1 Supplemental Decl. ISO Sur-Reply to MSJ of Invalidity, ¶ 14. The only authority Mitchell cited in the hearing to support this proposition was *Budde v. Harley-Davidson, Inc.* 250 F.3d 1369 (Fed.Cir.2001). In *Budde*, the Federal Circuit stated, "it is well settled that whether or not the specification adequately sets forth structure corresponding to the claimed function necessitates consideration of that disclosure from the viewpoint of one skilled in the art." *Id.* at 1376. While this is the law, the specification must disclose at least some kind of structure in the first place for this rule to apply. The law

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(Cont'd)

> **MR. SCHWARTZ:** Well, the structure has to do with the tri-state drivers. The tri-state drivers were known to those of ordinary skill in the art at the time this application —

In response, Intel states:

> **MR. VAN NEST:** Your Honor, there isn't a word anywhere in the specification about a tri-state driver.

is clear: the corresponding structure must appear in the specification, and an expert cannot use his knowledge to select a structure that is capable of performing the recited function. *Atmel*, 198 F.3d at 1382 ("knowledge of one skilled in the particular art . . . may only be employed in relation to structure that is disclosed in the specification."). This is the trade off for claiming as means-plus-function. The limitation must 'be construed to cover the corresponding structure . . . described in the specification and equivalents thereof.' " 35 U.S.C. § 112, ¶ 6. *Braun Med.*, 124 F.3d at 1424. Therefore, *some* structure must be identified.

Following the hearing on this motion, where Mitchell was unable to articulate a structure, Mitchell filed its Notice of Record Cite and Supplemental Authority (Docket No. 191). Despite the repeated inquiries for Mitchell to identify a structure, even in its supplemental briefing, Mitchell could point to no more than the "logical element" language above. Mitchell reurges the proposition that "[o]ne skilled in the art would know that the logical element, each of which can logically connect or disconnect, is the recitation of the structure of the switch means" and that one skilled in the art would know from the "plurality of logical elements" language that the first and second switch means are tri-state devices. Mitchell's Notice of Record Cite and Supplemental Authority at 6-7. However, again no where in the specification do the phrases "tri-state devices" or "tri-state circuitry" appear.

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While tri-state devices may perform the recited functions, and one skilled in the art might know the function could be performed by a tri-state device, the patentee is limited to structures actually disclosed in the specification when the patentee claims as means-plus-function. *See Atmel,* 198 F.3d at 1382. Here, no structure is disclosed in the specification for this function.

Mitchell points to a printing error in the patent office that caused part of a sentence to be deleted in column 14:22. The sentence in the patent reads "[t]he buffers driving the"; and the rest of the sentence is cut off. '154 patent, Col. 14:22. Mitchell argues that in reviewing the prosecution history, it is clear that the sentence at one time read "[t]he buffers driving the data bus lines have full 'three-state' capability. This is necessitated by the fact that the lines are bi-directional." Mitchell's Notice of Record Cite and Supplemental Authority at 5. Mitchell argues that this language is specifically directed towards the "three-state" capability and supports a corresponding structure. *Id.*

Even if this sentence is directed toward tri-state circuitry, and it is debatable that even the complete version of the sentence would support a corresponding structure, at no time did Mitchell file a certificate of correction to remedy this omission. The law requires the structure to be set forth in the specification, not the prosecution history. *See* 35 U.S.C. § 112, ¶ 6. It is the patentee's responsibility to review and correct errors in the patent in a timely fashion to avoid errors and omissions. *See Sw. Software, Inc. v. Harlequin, Inc.*, 226

F.3d 1280, 1296 (Fed.Cir.2000) ("Moreover, it does not seem to us to be asking too much to expect a patentee to check a patent when it is issued in order to determine whether it contains any errors that require the issuance of a certificate of correction."). The USPTO offers the certificate of correction procedure to cure just such defects so that patent owners can be assured that when the public views their patents, they view accurate representations of the claimed invention. *See id.* (In a case where the corresponding structure was not originally included in the patent, the Federal Circuit noted: "Until the PTO issues a certificate of correction pursuant to 35 U.S.C. § 254 adding the corresponding structure, such a claim would appear invalid to the public, and reasonable competitors would be justified in conducting their affairs accordingly.").

There is no reference to a structure in the specification to support the functions in limitations nine and ten as required by 35 U.S.C. § 112, ¶ 6; therefore, Claim 1 is invalid because it is indefinite.

Corresponding Structure for "means for causing"

The thirteenth and fourteenth limitations claim a "means for causing" with functions of "(1) [c]ausing said first and second switch means to remain in said non signal-conducting state upon application of power to said CPU power circuit and to assume a signal conductive state upon receipt of an appropriate signal from said CPU and (2) [a]ssum[ing] a non-signal conducting state upon receipt of an appropriate signal from said CPU."

Claim Construction Opinion at 33. In identifying the corresponding structure to these functions at the *Markman* hearing, Intel proposed adopting Judge Illston's previous construction. Mitchell did not provide the Court with an alternative corresponding structure in its brief or argument; therefore, the Court adopted Judge Illston's structure and stated "[t]o the extent that any structure for the corresponding function of the thirteenth and fourteenth limitations is provided in the specification, that structure is described at col. 24:67-col. 25:56." *Id.* The passage at columns 24:67-25:56 contains no structure. Rather, as discussed below, even Mitchell recognizes that the passage describes the operation of the switch means, but does not disclose any structure.

At the hearing, Mitchell referred the Court to a device called a MCS-6520 and said the device related to tri-state drivers. Hearing on Mot. Summary Judgment Tr. at 30. This device is discussed in column 15 and is completely outside the *Markman* ruling. '154 patent, Col. 15:42-55. Even if the Court considered the MCS-6520 as a possible structure, nothing in this part of the specification links the MCS-6520 with claim limitations thirteen and fourteen.[6] The MCS-6520 is a chip

6. The language reads:

> The MCS6520 is a direct pin for pin replacement for the Motorola MC6820 Peripheral Interface Adapter, the "PIA." As such, it meets all of the "PIA" electrical specifications and is totally hardware compatible with the MC6820.

(Cont'd)

comprised of various parts including drivers, but no driver is specifically detailed in the description at column 15. Intel argued, and Mitchell did not rebut the statement, that Mitchell is essentially saying that one skilled in the art would read the language at columns 24-25 and then look at the MCS-6520 as a whole and determine that somewhere in that chip is a tri-state device that is the structure for the functions of "means for causing."[7] Federal Circuit precedent simply does not allow this reading of the patent to satisfy the § 112, ¶ 6 requirement. *See Atmel,* 198 F.3d at 1382. Mitchell could

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(Cont'd)

> The MCS6520 is an I/O device which acts as an interface between the microprocessor and the peripherals such as printers, displays, keyboards, etc. The prime function of the MCS6520 is to respond to stimulus from each of the two worlds it is serving. On one side, the 6520 is interfacing with the peripherals via two eight-bit-bi-directional peripheral data ports. On the other side, the device interfaces with the microprocessor through an eight-bit data bus. . . ."

'154 patent, Col. 15:42-55.

7. **MR. VAN NEST:** What they are saying is you have to read this [Cols 24-25] and then go look at the 6520, which is a whole chip. It is not a switch or a buffer or a driver. It is a whole chip, Your Honor, with thousands and thousands of transistors. They are saying go look at this and somewhere in it you can find a tri-state driver and that is our structure.

Hearing on Mot. Summary Judgment Tr. at 31.

not identify any other possible corresponding structure at the hearing.[8]

In its post-hearing-supplemental briefing, Mitchell seems to abandon the MCS-6520 argument and instead lays out the entire passage the Court set out in the *Markman* opinion[9] and argues that the passage "is

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8. Hearing transcript at p. 33:

> **THE COURT:** So what is the structure that one of ordinary skill in the art would have seen and linked up to the function?
>
> **MR. SCHWARTZ:** Yes, Your Honor. That is precisely the point that Mitchell has taken in this case. **There is no specific detailed structure set out in the specification.**

9. The passage reads:

> Col. 24, line 67 to Col. 25, line 17:
>
> When power is removed from the BICPU microcomputer power circuits, a first switch means automatically, logically disconnects, and floats each connected circuit, and latches the first switch means in the logically disconnected position. Each logically disconnected and latched, floating, address circuit, data circuit and control circuit stays floating and logically disconnected and latched, when power is supplied to the BICPU microcomputer power circuits, until each first switch means is logically connected by signals from the BICPU microcomputer, after power is supplied to the BICPU microcomputer power circuits.

(Cont'd)

actually a description of the *operation* of the switch means." Mitchell's Notice of Record Cite and Supplemental Authority at 8 (emphasis added). Thus, Mitchell's reasoning is the same as its argument for limitations nine and ten: this passage does not identify a specific structure, but one skilled in the art would know that the corresponding structure could be the control elements of the tri-state devices. *Id.* ("What is set forth

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(Cont'd)

> A first switch means remains under control of the BICPU microcomputer, after power is supplied to the power circuits, and the BICPU microcomputer can logically disconnect and float, or logically connect, each of these circuits connected to a first switch means.

Col. 25, lines 33-49:

> Each of these circuits contains a second switch means, similar in action to the first switch means, except the logically disconnected, floating, latched portion of the circuit, is connected to the CPU of the BICPU microcomputer. Each logically disconnected, floating, latched CPU address circuit, data circuit and control circuit, stays floating and disconnected and latched, when power is supplied to the BICPU microcomputer power circuits until each second switch means is logically connected, by signals from the BICPU microcomputer after power is supplied to the BICPU microcomputer power circuits.
>
> A second switch means remains under control of the BICPU microcomputer, after power is supplied to the power circuits,. and the BICPU microcomputer can logically disconnect or logically connect, each of the circuits connected to a second switch means.

above in Columns 24 and 25 to one skilled in the art is a description of how control is exerted on the control elements of the tri-state devices."). Mitchell asserts that the "means for causing" is understood by one skilled in the art as a specific portion of the tri-state circuitry, which is the control element. *Id.* But again, there is no reference to tri-state circuitry, control elements, or any other structure in this passage.

Once again, there is no reference to a structure in the specification to support the functions in limitations thirteen and fourteen as required by 35 U.S.C. § 112, ¶ 6, thus Claim 1 must fail as invalid because it is indefinite.

CONCLUSION

Accordingly, Mitchell has failed to raise a fact issue as to whether limitations nine, ten, thirteen, and fourteen set forth corresponding structures for their functions as required by 35 U.S.C. § 112, ¶ 6. The Court holds that Claim 1 is indefinite and therefore invalid as a matter of law and **GRANTS** Intel's motion for summary judgment as to invalidity.

So ORDERED and SIGNED this 22nd day of November, 2006.

s/ Leonard Davis
LEONARD DAVIS
UNITED STATES DISTRICT JUDGE

APPENDIX C — DECLARATION OF JOHN D. PATTERSON, PH.D. IN SUPPORT OF OPPOSITION TO INTEL'S MOTION FOR SUMMARY JUDGMENT OF INVALIDITY, DATED AUGUST 10, 2006

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

CIVIL ACTION NO.
2:04CV-450 LED

Judge: Hon. Leonard Davis
Date Complaint Filed: 12/17/04
Trial Date: 10/10/06

MAURICE MITCHELL INNOVATIONS, L.P.

Plaintiff,

v.

INTEL CORPORATION

Defendant.

DECLARATION OF JOHN D. PATTERSON, PH.D. IN SUPPORT OF OPPOSITION TO INTEL'S MOTION FOR SUMMARY JUDGMENT OF INVALIDITY

Appendix C

John D. Patterson hereby declares as follows:

1. I have been retained on behalf of plaintiff Maurice Mitchell Innovations, LP (Mitchell) in the above-captioned matter to serve as a technical expert relating to Mitchell's claims of infringement by Defendant Intel Corporation (Intel) of U.S. 4,875,154 (the '154 patent).

2. I have also been retained on behalf of plaintiff Mitchell in the above captioned matter to serve as a technical expert relating to Intel's defense that Claim #1 of the '154 patent is invalid.

3. I confirm the statements in my rebuttal expert report on invalidity that the '154 patent is, in fact, valid and that the statements I have made on pages 55 through 59 with respect to the fact that sufficient disclosure is contained in the written specifications of the '154 patent. That is, the specification and drawing of the patent provide sufficient disclosure to one skilled in the art what structure is used for the switch means of elements 9 and 10 of the claim as interpreted by the Court. Also, there is sufficient disclosure to one skilled in the art what structure is used to perform the function of the elements 13 and 14 of the claim which call for [13] "means for causing" said first and second switch means to remain in said non-signal conducting state upon application of power to said CPU power circuit and to assume a signal-conductive state upon

receipt of an appropriate signal from said CPU, and to [14] assume a non-signal conducting state upon receipt of an appropriate signal from said CPU".

4. With respect to the first switching means, and the second switching means, support for the switch means is disclosed in Col. 19, Line 64 — Col. 20, Line 5, which states that "each first switch means and second switch means actually represents a plurality of logical elements, each of which can logically connect, or logically disconnect an address, data or control circuit that is mechanically connected to the switch means under the control of the CPU 102 when power is being supplied to the BICPU microcomputer power circuits."

5. One skilled in the art at the time of the invention would have known that tri-state circuits are such logical elements which can logically connect or logically disconnect as described in the specification of the '154 patent. Tri-state devices were well known at the time that the patent application was filed by Mitchell. As an example of the use of tri-state devices and the knowledge of a person of ordinary skill in the art at the time Mitchell filed his patent application, is the type MCS6520 peripheral interface adapter (PIA) Mitchell referred to and incorporated by reference in the specification of the patent.

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6. With respect to the "means for causing said first and second switch means to remain in the non-signal conductive state upon application of power to the CPU circuit and to assume a signal conductive state upon receipt of an appropriate signal from the CPU and to assume a non-signal conductive state upon receipt of an appropriate signal from the CPU", one skilled in the art would understand from the description of the function that it refers to the application of a signal to the control element (such as an enable terminal) of a tri-state circuit caused by a signal from the CPU.

7. The disclosure showing this specific structure in the '154 patent specification is found in the teaching of the use of the MCS650X as the disclosed exemplary CPU. This CPU was well known at the time of the invention and extensive technical support for facilitating its use and that of known substitutes, such as the MC6800 MPU and its corresponding PIA, the MC6820, was available to those skilled in the art.

8. As shown in Col. 54, lines 67 - Col. 55, line 1, the '154 patent points out that Fig. 19 is an overall drawing of a BICPU microcomputer 400 adapted from a conventional microcomputer of the MCS650X chip family, which includes the MCS6502 MPU and a MCS6520 PIA and which are respectively pin-compatible with the MC6800 MPU/MC6820 PIA mentioned above. See Col. 15, lines 42-55 of the '154 specification.

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9. The recitation goes on to further state that the "MCS6520 is an input/output device which acts as an interface between the microprocessor and the peripherals such as printers, displays, keyboards, etc. The prime function of the MCS6520 is to respond to stimulus from each of the two worlds it is serving. On the one side, the 6520 is interfacing with the peripherals via two eight-bit bi-directional peripheral data ports. On the other side, the device interfaces with the microprocessor through an eight-bit data bus."

10. Further, the knowledge of one skilled in the art when interpreting the statement at col. 15, lines 61-63: "no external logic is required for interfacing the MCS650X microprocessor to most peripheral devices" would be sufficient to determine that the structure of the "means for causing" provided by the interface circuits containing tri-state devices is taught by the referenced technical description of the MCS6520 PIA, which was well known to persons of ordinary skill in the art at the time of the invention. Thus, to one skilled in the art this means there is a chain of causality supplying the "means for causing" from the microprocessor that runs the programs implementing Mitchell's invention through to the tri-state logic in other systems connected to the system bus-circuits, which go into and out of their high impedance states when appropriate control signals are applied to a control pin. This passage starting

in Col. 15 confirms and corroborates what one skilled in the art would understand from Col. 24, line 67 through Col. 25, line 56 of the '154 patent.

11. That is, based upon the description of the operation of the first and second switch means and the functions for the "means for causing" specified in Col. 24 line 67 through Col. 25 line 56 in the '154 patent specification, it is clear to one skilled in the art what the structure is that is required to perform the functions in the specification of the patent.

12. It should also be noted that Mitchell, in the '154 patent refers to the MCS6500 microcomputer family hardware manual which shows what one skilled in the art would have understood at the time of the invention. In the manual, there are contained many descriptions of the operation of the MCS6502 microprocessor. This shows how the CPU can provide signals which control high impedance, three state capability and direct transistor drive peripheral lines. See, e.g., Section 1.5.3.1 on page 56 of this hardware manual for a discussion of the 8 bit bidirectional data bus which allows the transfer of data between the microprocessor and the MCS6520: "The data bus output drivers are 3-state devices that remain in the high impedance state except when the microprocessor reads data from the peripheral adaptor. This data bus is the same as discussed in Section 1.3.1, "Bus Structure."

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13. One skilled in the art would have understood at the time of the '154 application that the circuitry disclosed in the hardware manual is exemplary of what would be used for the "means for causing" the lines to come out of the high impedance (nonconductive) state. (See 2.3.4.2 of the *Moore* reference.)

14. Accordingly, the very circuitry shown in the exemplary device referred to by Mitchell shows that the circuitry for connecting the CPU to the control elements of the tri-state device are well known to one skilled in the art. Thus, one skilled in the art would have understood the structure of the "means for causing" given the specification of the Mitchell patent and the disclosures contained therein.

15. I have studied the Declaration of Roderick Swift attached as Exhibit G of defendant Intel's Motion for Summary Judgment for invalidity and I agree, confirm and incorporate by reference the statements made by Dr. Swift in paragraphs 10 - 35 of the Declaration.

16. These statements made by Dr. Swift are fully in accord with what I have stated in the rebuttal expert report on invalidity that was submitted to the court on July 21, 2006.

17. I further state that nothing in the Declaration of Dr. Swift in any way contradicts or modifies

any of my statements in the report nor do any of my statements contradict any of the statements in the report of Dr. Swift. To one skilled in the art, both reports say the same thing with respect to the structure disclosed in the '154 patent for limitations 9, 10, 13 and 14, but with different language in a different way.

18. With respect to the fact that I cited a passage at Col. 15, it is to explain that the peripheral interface adapter known as the MCS6520 is an example of a circuit device that was a well known use of tri-state circuits. One skilled in the art would understand how such circuitry was constructed and how it operated. The description of the functions of the means for causing in limitations 13 and 14 is a description of the function of the first and second switch means. That is what is described in Col. 24, line 67 to Col. 25, line 56. One skilled in the art would understand the structure of switch means that is used for the means for causing in limitations 13 and 14 of the claim is the control element structure taught by the tri-state devices of the MCS6520 which as set forth above, are examples of the tri-state logic circuit structure. The citing of the MCS6520 alone would be sufficient to one skilled in the art that the MCS6520 teaches the tri-state circuitry that is the structure for elements 9 and 10 of the claim and that the control elements of the MCS6520 tri-state circuits are the "means for causing" of elements 13 and 14.

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FURTHER, DECLARENT SAYETH NOT.

I declare under penalty of perjury that the foregoing is true and correct.

s/ John D. Patterson
JOHN D. PATTERSON

Date: August 10, 2006.

APPENDIX D — ORDER OF THE UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT DENYING PETITION FOR REHEARING, FILED NOVEMBER 5, 2007

UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

2007-1108

MAURICE MITCHELL INNOVATIONS, L.P.,

Plaintiff-Appellant,

v.

INTEL CORPORATION,

Defendant-Appellee.

ORDER

A combined petition for panel rehearing and for rehearing en banc having been filed by the Appellant, and the petition for rehearing, having been referred to the panel that heard the appeal, and thereafter the petition for rehearing en banc having been referred to the circuit judges who are in regular active service,

UPON CONSIDERATION THEREOF, it is

ORDERED that the petition for panel rehearing be, and the same hereby is, DENIED and it is further

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ORDERED that the petition for rehearing en banc be, and the same hereby is, DENIED.

The mandate of the court will issue on November 13, 2007.

Circuit Judge Schall did not participate in the vote.

FOR THE COURT,

s/ Jan Horbaly
Jan Horbaly
Clerk

Dated: 11/05/2007